FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1778.0180000	09/925,314
APPLICANT: Christopher R. Risucci	
FILING DATE: August 10, 2001	GROUP: 2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	5,632,024	05/1997	Yajima *et al.*			
	AB1						
	AC1						
	AD1						
	AE1						
	AF1						
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AR	1	*MIPS Technologies Licenses MIPS64™ 5Kf™ and MIPS32™4KEc™ Processor Cores to LSI Logic*, from http://www.mips.com/pressReleases/061101C.html, MIPS Technologies, Inc., 3 pages (June 11, 2001).
AS	1	Sweetman, D., *See MIPS Run*, Morgan Kaufmann Publishers, Inc., ISBN 1-55860-410-3, pp. vii-xiv, 91-101, 369-386 and 423-425 (1999).
AT	1	Turley, J., "LSI's TinyRisc Core Shrinks Code Size: Code-Compaction Technique Squeezes MIPS Instructions Into 16 Bits," *Microprocessor Report*, Microdesign Resources, pp. 40-43 (October 28, 1996).

EXAMINER: [signature] DATE CONSIDERED: 12/16/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2						
	AB2						
	AC2						
	AD2						
	AE2						
	AF2						
	AG2						
	AH2						
	AI2						
	AJ2						
	AK2						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2					–	Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

27	AR	2	*LSI Logic announces world's highest-performing 64-bit MIPS embedded microprocessor core: Two new MIPS-based EasyMACRO ASIC cores offer size, speed and performance advantages for a broad range of applications*, from http://www.lsilogic.com/news/product_news/pr20000605.html, LSI Logic Corporation, 2 pages (June 5, 2000).
	AS	2	
	AT	2	

EXAMINER	DATE CONSIDERED 5/27/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.